Attachment B: Explanation of Attachment A

Attachment A contains part of the verilog representation of the design of a portion of an integrated circuit controller chip that was developed prior to March 2, 1998. The chip design corresponds to all parts of Figure 2 except the 7 physical pads along the top, and the bottom region labeled Memory core that is represented by a second integrated circuit chip not included in this attachment. Four modules are included in Attachment 1: top_unit (lines 1-475), top_lgc (line 476-738), cmd_unit (lines 739-1102), and cmd_ctrl (lines 1103-1686).

top_unit is the top level representation of a portion of chip. All of the signal names in lines 4-10 represent top level signals on the chip. Some of them are physical pads (either corresponding to the 7 signals of Figure 2 or to pads leading to the memory chip). Included in this group is CLK and SPI_CSB. RESET_IN comes from a vendor supplied and proprietary power-on reset module that produces a positive level when power is stable on the chip and processing can safely begin. It is initially 0 until a short time after power is stable, then switches to 1 and remains in this state during normal powered operation falling to 0 when power drops below a safe level. top_unit consists of an instantiation of 6 lower level modules: top_lgc (line 241), cmd_unit (line 263), cont_unit (line 319), data_unit (line 385), reg_unit (line 427), and bus_cont_unit (line 457). Of these modules, only top_lgc and cmd_unit are of interest for determining mode selection. Note that on line 4, 8, 16, 17, & 30, signals CLK, RESET_IN and SPI_CSB are all inputs to this top level module.

top_lgc is an HDL description of the logic block. On lines 487 & 529, SR_3 is an output of this block. It is set in lines 602-616 from top level input RESET_IN, and is synchronized to transition from 0 to 1 at a positive edge of CLK three cycles after the start of RESET_IN.

cmd_unit consists of instantiation of 5 lower level modules: cmd_sr (line 964), cmd_lgc (line 981), cmd_ctl (line 1039), cmd_response (line 1073), cmd_crc (line 1093). Of these modules, the only one of interest is cmd_ctl.

cmd_ctl, like top_lgc, is an HDL description of the design. Logic designers document and simulate their design using this form of description. When they are satisfied with the results, they synthesize their design into a specific vendors logic library using commercially available software, generating a netlist showing the specific primitive units such as NAND and NOR gates, and flip flops of various kinds needed to implement the design as well as the interconnections between these units.

On line 1120-1121, signals SPI_MODE and SPI_CSB are shown as passing into or out of this module. On line 1155 SPI_MODE is declared as an output, meaning this module determines its state, and on line 1159 SPI_CSB is declared as an input. Referring to line 8 we see that SPI_CSB is an input to the chip, but SPI_MODE is not included in the list of top level inputs (line 4-10) meaning it is an internal signal. It is used throughout the chip to determine if we should operate in SPI mode or in MMC mode.

Referring to lines 1672-1679 we see how SPI_MODE is determined. Initially it is set to 0 because SR_3 starts at 0 (~SR_3 is 1). But when SR_3 becomes 1, the second test is performed. If PRE_GO_IDLE is 1 and SPI_CSB (input to the chip) is 0 then SPI_MODE is set to 1. To determine the value of PRE_GO_IDLE, refer to line 1426 where we check the status of `GO_INACTIVE_STATE, a verilog abbreviation for CMD0 (GO_IDLE_STATE, or host reset command). If that command is the currently active command (as decoded by the command logic contained in HDL module cmd_lgc, not included in Attachment A), then NS (next state) is assigned the value GO_IDLE_S, and control transfers to GO_IDLE_S (lines 1525-1528) where PRE_GO_IDLE is set to 1. At this time SPI_CSB determines how SPI_MODE will be set. During the next command decoding, PRE_GO_IDLE goes to 0 (line 1309) and this mode test is never performed again until the card is power cycled and a new CMD0 is issued by the host. Thus if an SPI host asserts SPI_CSB low during transmission of CMD0 the card will enter SPI mode, while if an MMC host does not assert this pin low the chip will not enter SPI mode but will stay in MMC mode.